



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

mf

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/629,112	07/29/2003	Junichi Sakamoto	09812.0498-00000	6984

22852 7590 02/23/2007
FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER
LLP
901 NEW YORK AVENUE, NW
WASHINGTON, DC 20001-4413

EXAMINER

WOODS, ERIC V

ART UNIT	PAPER NUMBER
----------	--------------

2628

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/23/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

10/629,112

Applicant(s)

SAKAMOTO ET AL.

Examiner

Eric Woods

Art Unit

2628

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 13 November 2006.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-12 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 1/26/2007 was filed after the mailing date of the Non-Final Rejection on 8/10/2006. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the examiner is considering the information disclosure statement.

It is noted that no translations were provided for documents JP 59-177651 and JP 63-195780. Therefore, while the abstracts were considered, the document as a whole was not. Therefore, those references were not marked as considered, particularly in light of the fact that applicant provided machine-translated versions of the other three documents in question.

It is noted that the Inoue et al publication (JP 10-293853) has a US equivalent of US 5,982,380 (Inoue et al) that will be used as below, wherein such documents are regarded as materially equivalent with respect to provision by applicant under 37 CFR 1.97(b) and (c).

Response to Arguments

Applicant's arguments, see Remarks pages 1-6 and claim amendments, filed 11/13/2006, with respect to the rejection(s) of claim(s) 1-12 under various statutes have been fully considered and are partially persuasive.

Specifically, the rejections of claims 1-12 under 35 USC 112, second paragraph, stand withdrawn. Applicant has amended to correct the cited deficiencies.

Art Unit: 2628

The amendment to correct the deficiency that led to the previous rejection of the claims under 35 USC 112, second paragraph, has materially changed the scope of the claims.

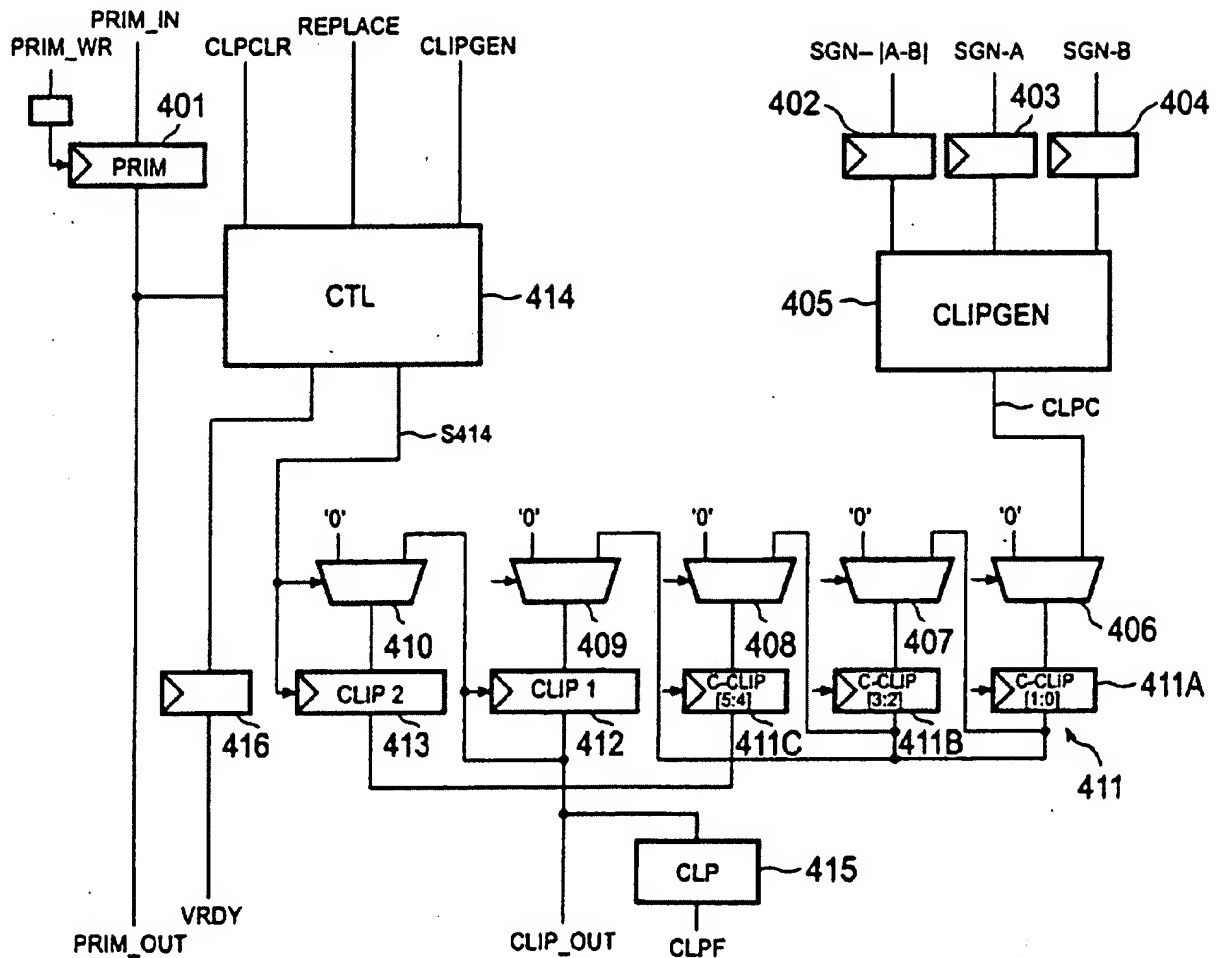
The rejections of claims 1-12 under 35 USC 103(a) do not stand withdrawn.

Applicant's arguments are not found to be persuasive. The main point of contention in the rejection under 35 USC 103(a) is the limitation "Clip registers cascade connected to an output of said current clip register for replacing the held data with the clip codes held by the register of a previous stage".

That recitation is the focus of the arguments on pages 8-10 (applicant's numbering). Negishi is not relied upon for cascaded clip registers *per se* and thus is not relevant to this discussion, thusly mooted pages 8 and 9. Instead, *Inoue* is the reference in question.

Firstly, it is instructive to refer to applicant's description of an embodiment (Figure 3) in drawing format:

FIG. 3



Now, note applicant's written description (quoting from the Pre-Grant Publication form of the instant application):

[0054] A clipping device 400 has, as shown in FIG. 3, a primitive register (PRIM) 401, input registers 402 to 404, a clip code generation circuit (CLIPGEN) 405, multiplexers (MUX) 406 to 410, clip registers 411 (A, B, C), 412, and 413 each consisting of 6 bits, a controller (CTL) 414, a logic circuit (CLP) 415, and an output register 416.

Art Unit: 2628

[0113] Therefore, in the present embodiment, in order to secure 3 vertexes' worth of capacity when the capacity of the clip register is one triangle's worth, a 6-bit clip register (CLIP1) 412 and a 6-bit clip register (CLIP2) 413 are provided in addition to the clip register 411 and the three vertexes' worth of capacity is made 18 bits.

[0114] The clip register (CLIP1) 412 shifts the content of the 6 bits of the clip register 411 via the multiplexer 409 in accordance with the control signal S414 of the controller 414 and outputs the shifted content to the logic circuit 415 and the processing circuit of the following stage.

[0115] The clip register (CLIP2) 413 shifts the content of the 6 bits of the clip register 412 via the multiplexer 410 in accordance with the control signal S414 of the controller 414 and outputs the shifted content to the logic circuit 415 and the processing circuit of the following stage.

[0164 (in part)] As explained above, according to the present embodiment, since provision was made of a clip code generation circuit 405 for generating clip codes obtained by setting data in accordance with results of comparison of vertex coordinates of a triangle primitive and a judgment reference value of a multi-dimensional region and a negative value of the judgment reference value as bit data for the vertexes of the primitive; a current clip register 411 for shifting the clip codes generated at the clip code generation circuit 405 in accordance with a control signal; clip registers 412 and 413 **cascade connected** to the output of the current clip register and able to replace the clip codes in accordance with a control signal; (emphasis added)

The definition of the word 'serial' in the computer hardware industry is a series connection; that is, something 'of, forming, or arranged in a series' or 'of or relating to the sequential performance of multiple operations' (specific computer science domain definition (American Heritage College Dictionary)). That is, one item connected after another. Applicant uses the term 'cascade connected' in the claim.

The definition of cascade (American Heritage College Dictionary) is a succession of stages, processes, operations, or units, with an *electronics*-specific definition of "A series of components or networks, the output of each of which serves as the input for the next."

That is, the words are synonymous, and a closer comparison of the system of *Inoue* and that of applicant reveals that the recited register connections are in fact the same.

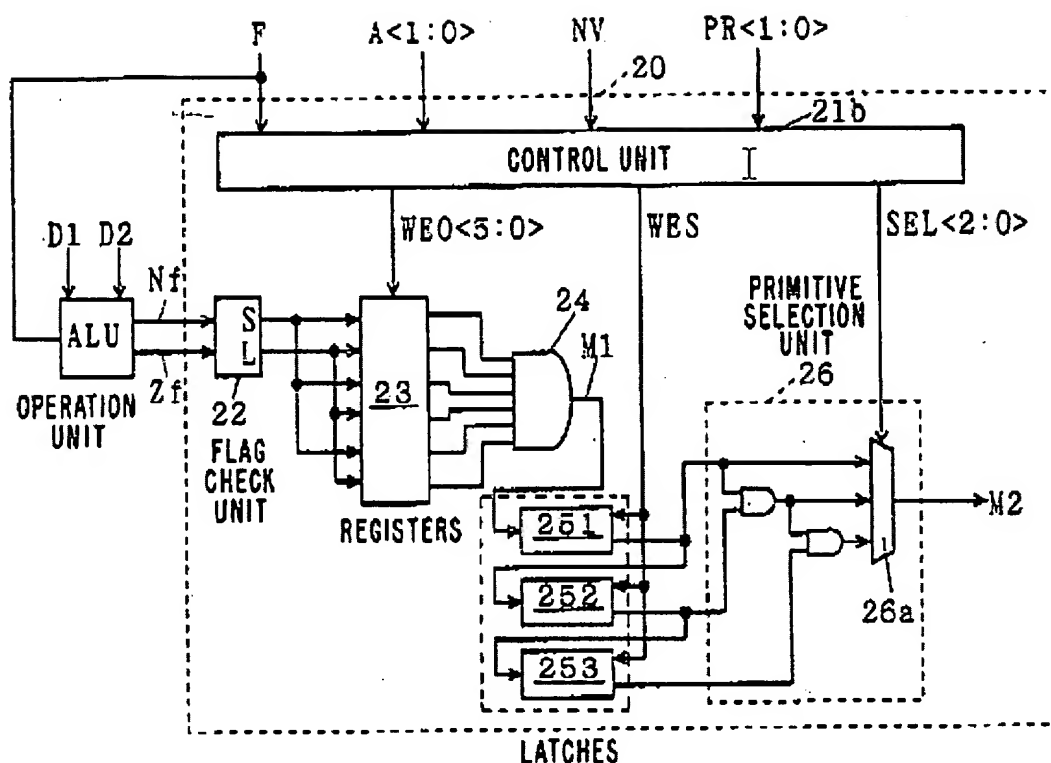
Applicant's system shifts values in the registers as in $A \rightarrow B \rightarrow C$ format (411 \rightarrow 412 \rightarrow 413) as explained above.

However, applicant takes the position below in the Remarks filed 11/13/2006 with respect to the *Inoue* reference (applicant page numbered 10, first paragraph, quoting from *Inoue*): "Moreover, latches 251-253 'are connected in series and a shift signal WES controls input/output of data. When the shift signal WES is activated, data stored in the latches 251 to 253 are shifted in this order' (8:11-14 and Fig 6). Data stored in the latches may be shifted. However, this does not teach or suggest the claimed 'clip registers cascade connected ...' as recited in claim 1."

This position is clearly erroneous, as shifting data through serially connected latches is the same thing as shifting data through cascade-connected registers, since both elements are doing nothing but holding the results of calculations, and they are both memories. Applicant does not contest that.

Applicant has clearly conceded that *Inoue* has latches 251-253 that are connected in series (Figure 6 below).

F I G . 6

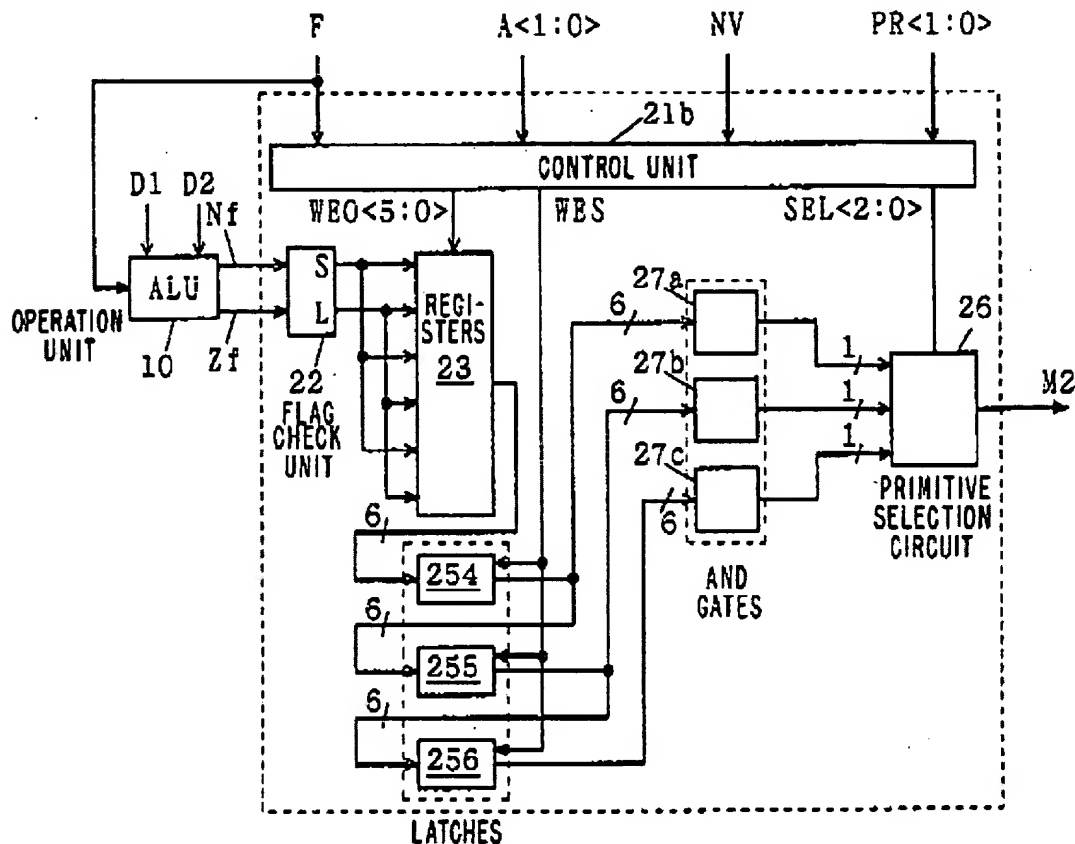


Inoue describes these latches as follows: "In the third preferred embodiment, latches 251 to 253 and a primitive selection unit 26 are additionally provided to the clip-code generation/judgment unit 20 of the first preferred embodiment... The latches 251 to 253 are connected in series and a shift signal WES controls input/output of data. When the shift signal WES is activated, data stored in the latches 251 to 253 are shifted in this order... In other words, the judgment signals M1 on the respective vertices constituting the primitive are **sequentially** stored in the latches 251 to 253..." (8:1-60). That is to say, the data is transferred from the registers to the latches. However, to avoid a

Art Unit: 2628

discussion on equivalency, for purely purposes of clarification, examiner now provides

Inoue Figure 8:



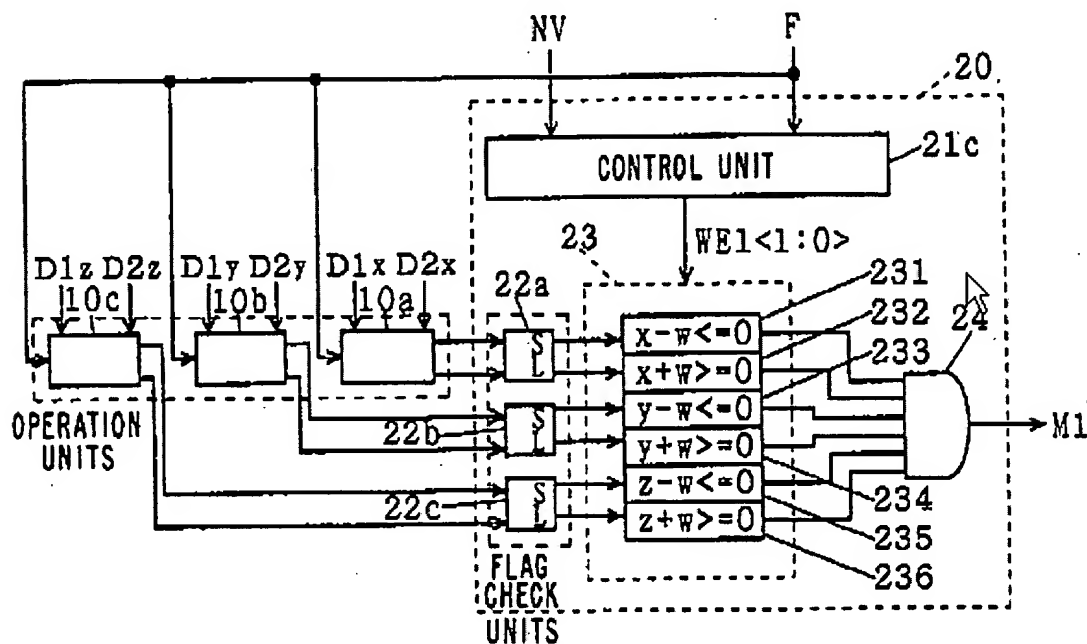
Note the description for this structure (Inoue 8:64-9:8):

"FIG. 8 is a circuit diagram showing a modification of the third preferred embodiment of the present invention. Without provision of the 6-input AND gate 24, the 6-bit output from the group of registers 23 is inputted to a 6-bit latch 254. From the latch 254 to the latch 256, data to be stored therein are shifted according to the shift signal WES, like the latches 251 to 253. Six-input AND gates 27a to 27c obtain the logical products of the values stored in the latches 254 to 256, respectively, and each output 1-bit signal to the primitive selection unit 26. Unlike the first preferred embodiment, the above configuration may be adopted since the judgment signal M1 is not necessarily needed."

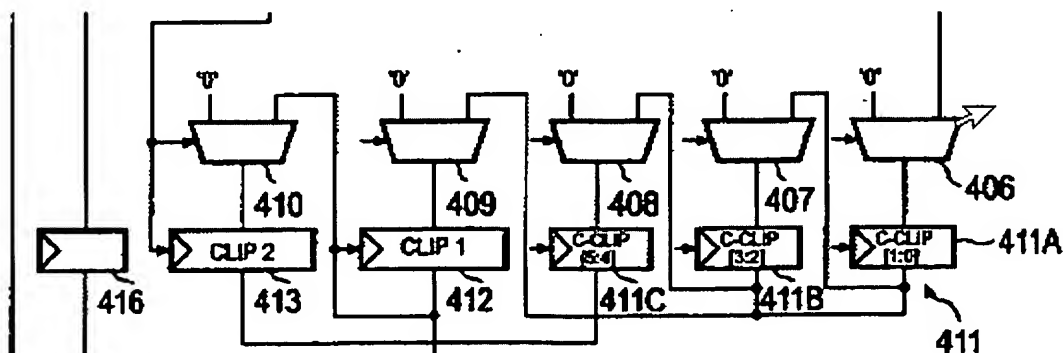
Art Unit: 2628

Finally, note Inoue Abstract: "It is judged that a vertex exists within a view volume when values stored in registers (231 to 236) are all "1". In other words, whether the vertex exists within or beyond the view volume can be judged by whether the values stored in the registers (231 to 236) are all "1" or not."

Wherein Registers 23 are composed as follows, as in Figure 4:



Finally, applicant's own registers 411-413 contain clip codes as above (excerpted from applicant Figure 3 above):



Art Unit: 2628

[0102] The clip register 411 functions as the current clip register (C-CLIP) and shifts 2 bits of the judgment results of $A < -B$ and $A > B$, that is, the clip code CLPC, when the CLIPGEN_A,B instruction is executed.

[0103] When executing the CLIPGEN instruction three times, specifically, when continuously executing CLIPGEN_X,W, CLIPGEN_Y,W, and CLIPGEN_Z,W when A is the coordinate of the three axes X, Y, and Z and B is the judgment reference value W, the values of the 6 bits of the clip register 411 become as shown in FIG. 8 and the following:

[0104] bit5: $(X < -W)?1:0$

[0105] bit4: $(X > W)?1:0$

[0106] bit3: $(Y < -W)?1:0$

[0107] bit2: $(Y > W)?1:0$

[0108] bit1: $(Z < -W)?1:0$

[0109] bit0: $(Z > W)?1:0$

[0110] Namely, the judgment result 1 or 0 of $X < -W$ is shifted to the bit 5, the judgment result 1 or 0 of $X > W$ is shifted to the bit 4, the judgment result 1 or 0 of $Y < -W$ is shifted to the bit 3, the judgment result 1 or 0 of $Y > W$ is shifted to the bit 2, the judgment result 1 or 0 of $Z < -W$ is shifted to the bit 1, and the judgment result 1 or 0 of $Z > W$ is shifted to the bit 0.

That is to say, as the final result of the above, Inoue's Registers 23 contain the same 6-bit information as the "current clip register" of applicant, that is, they both contain the same results from the same logical operations on the same variables.

Furthermore, when compared to Figure 8, it can be clearly seen that the information in registers 23 are serially transferred through latches 254-256, which are known to be 6-bits wide as described above.

Therefore, it can be seen that applicant's assertion that the method of operation of *Inoue* was different than that in the instant specification was mistaken. Both systems utilize serially connected registers containing the same data (that is, especially when *Inoue* Figure 8 is considered).

Applicant's position is clearly shown to be error since the data held in the recited registers is the same information. Applicant has failed to rebut the *prima facie* case previously set forth by the Office. Therefore, for at least the above reasons, examiner's rejection of claims 1-12 under 35 USC 103(a) should be upheld.

Drawings

The drawings are objected to under 37 CFR 1.83(b) because they are incomplete. 37 CFR 1.83(b) reads as follows:

When the invention consists of an improvement on an old machine the drawing must when possible exhibit, in one or more views, the improved portion itself, disconnected from the old structure, and also in another view, so much only of the old structure as will suffice to show the connection of the invention therewith.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application.

Specifically, in Figure 3, the written description filed on 03/21/2005 (corrected) describes the data line between register 411 (page 18, [0111]) as follows: "The current clip registers 411A to 411C, that is, the current clip registers 411, output the 6-bit output to the multiplexer 409..." The drawings do not support this. The data line connecting registers 411A, 411B, and 411C to multiplexer 409 [0111] only show dots (connections) between the outputs of 411A and 411B, but not 411C. Such a bus could only therefore

Art Unit: 2628

be 4 bits wide, not the recited 6 bits. Thusly, the connection between that bus and 411C needs to be illustrated.

Any amended replacement-drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the examiner does not accept the changes, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6 and 11-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Inoue et al (US 5,982,380 A).

As to claims 1 and 5, (system that has circuitry that performs the following elements performs aforementioned clipping method in hardware (see Inoue 6:30-35); thusly, rejection against claim 1 equally valid against claim 5 (hardware-implemented method))

A clipping device for judging whether or not vertices expressed by a predetermined coordinate system are inside or outside a multi-dimensional region of an object to be drawn, comprising: (Inoue, Abstract; 2:20-40)

-A clip code generation circuit for generating clip codes obtained by setting data in accordance with results of a comparison of coordinates of said vertices and a judgment reference value of said multi-dimensional region and a negative value of the judgment reference value as bit data; (Inoue Figure 8: ALU 10 is provided with a value that represents a coordinate (X, Y, Z) of a point / vertex of a primitive (D1) and an absolute value W of one of the clipping planes (D2), as well as a signal indicating whether it should perform subtraction or addition (F) (4:55-67). This generates two resultant flags (Nf, Zf) that pass to flag check unit 22, which generates two outputs (S, L) that are passed (5:1-34) to one of the specific registers 231-236 in register 23 (6-bits wide, 6 individual 1-bit registers 231-236) based on the write enable (WE-6 bit) signal (5:34-51). These represent 'clip codes'. Circuit 20 is a clip code generation/judgment unit (6:22). Applicant's recited clip codes are defined and explained above (Response to Arguments). Applicant's clip codes are comparable to / are the same as the clip code / intermediate values held in Registers 23 of Inoue, as explained above.)

Art Unit: 2628

-A current clip register for shifting the clip codes generated at said clip code generation circuit; (Inoue Registers 23, Figure 8)

-Clip registers cascade connected to an output of said current clip register for replacing the held data with the clip codes held by the register of a previous stage; and (Inoue Figure 8, 8:65-9:7, latches 254-256 (comparable to latches 251-253 in Figure 6, which are described in 8:9-15 as "The latches 251 to 253 are connected in series and a shift signal WES controls input/output of data. When the shift signal WES is activated, data stored in the latches 251 to 253 are shifted in this order." Serially connected latches are comparable to cascade connected registers. This point has been extensively discussed, with attendant drawings, in the Response to Arguments section above, the entirety of which is hereby incorporated by reference.))

-A logic circuit for performing a logic operation with respect to all bit data set in said clip registers and setting a clip flag indicating whether or not a vertex to be judged is inside or outside the multi-dimensional region of the object to be drawn. (Inoue Figure 8, AND gates 27a-27c ('logic circuits') with respect to all data in said clip registers (6 bit-wide bus connections passing to 6-bit wide AND gate, 9:3-5) which output a resultant 1-bit signal to the primitive selection unit 26, wherein this 1-bit signal represents the clip flag (whichever one of the three signals is chosen by primitive selection unit 26 – 8:45-63))

Inoue thusly teaches all the limitations of the above claim. See Response to Arguments (incorporated by reference in its entirety).

As to claims 2 and 11, Inoue operates upon a three-dimensional view volume ('plurality of coordinate axes' 'predetermined coordinate system')(Table 1, Figures 13,

Art Unit: 2628

15-16, 1:29-63, Figure 1) and compares vertices / points ((2:20-41), Figures 1, 4, 6, 8). It generates 'a plurality of clip codes corresponding to the coordinate axes' ((ALU 10 + Flag Check unit 22 – 4:55-6:35), see Figure 1, illustrated coordinate axes comparison (registers 231-232: x-axis, registers 233-234: y-axis, registers 235-236: z-axis)), wherein registers 23 (Figure 1) and latches 254-256 (Figure 8, 8:64-9:3) are 6 bits wide, which clearly 'have a capacity for holding at least said plurality of clip codes'.

As to claims 3 and 12, reference Inoue teaches the use of absolute values in clipping preprocessing circuits, specifically 2:19-41 teaches that the clipping device performs an operation (subtraction) on the absolute value of a vertex coordinate and a pair of boundaries, wherein similar to applicant's diagrams the clip data of the boundaries are put into the register and the check is performed, and the code data recited by applicant clearly is stored (from the axis basis). Further, Table 1 in Inoue illustrates (1:53-63) how codes are created for the view volume, and Figure 1 illustrates how the code data is generated, etc, with Figure 8 illustrating the clip code generation mechanisms with ALU 10 and Flag Check unit 22.

As to claim 4, this is claim 3 made dependent upon claim 2. Clearly, the rejection of claim 2 applies therefore to this claim and is incorporated by reference in its entirety.

As to claim 6, see Figure 8. The primitive selection unit 26 takes on different values based on the type of primitive (8:45-63), wherein the vertex / register processing is done in accordance with the primitive type (vertex, line polygon), as in the cited text above, and resultant M2 signal is output.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-6 and 11-12 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Negishi et al (US Patent 6,005,590 A)('Negishi') in view of Inoue (US 5,982,380 A).

As to claim 1,

A clipping device for judging whether or not vertices expressed by a predetermined coordinate system are inside or outside a multi-dimensional region of an object to be drawn, comprising: (Negishi, Abstract, 1:5-2:20)

-A clip code generation circuit for generating clip codes obtained by setting data in accordance with results of a comparison of coordinates of said vertices and a judgment reference value of said multi-dimensional region and a negative value of the judgment reference value as bit data; (Negishi in Figure 3 teaches a clip code generating circuit, where FPU (floating point units) 103, 104, and 105 generate clip codes (7:52-8:15) that

Art Unit: 2628

then are passed to shift registers 304, 305, and 306. As set forth (7:52-8:15) by Negishi, the clip codes are generated by comparing the coordinates of the vertices and the reference values (e.g. $X=X_{MAX}$ and $X=X_{MIN}$) for comparison through the clipping region (which prima facie is multi-dimensional (see Figures 5-7 and the explanations provided in the cited references, and these are clearly bit data since they are in the memory of a digital computer. It would be obvious, as shown in Figure 6 and further explained in 8:64-10:7, that each vertex is processed on its own, which teaches vertices, and the recited 'judgment values' are merely the bounding coordinates of the clipping region and/or the guardband. Negishi also generates clip state codes (see Figure 7, 8:45-65), where these state codes indicate whether an object is inside, outside, or intersects the specific view volume. These codes can be taken to embody positive and negative judgment values as required by the claim, since they indicate where the object is, and specific information with relation to the vertex)(Inoue generates clip codes in Figure 7, with the those codes propagating through several layers of registers, as shown in elements 251-253, which constitute registers)

-A current clip register for shifting the clip codes generated at said clip code generation circuit; (Negishi - the resulting clip codes from FPU 103, 104, and 105 are then sent to shift registers 304, 305, and 306 which are comparable to applicant's "current clip registers". The results are then passed on to generic clip code register 308. The system works as specified above (8:48-64). Further, Negishi's shift registers clearly move data from each shift register to the next to the final clip code register at the bottom

– see 8:45-65, so clearly they constitute shift registers)(Inoue, registers 23 in Figure 8 for example)

-Clip registers cascade connected to an output of said current clip register for replacing the held data with the clip codes held by the register of a previous stage; and (Negishi clearly shows clip registers 304-306, which constitute 'clip registers cascade connected' as recited above, and the clip code register 308 would then constitute 'clip registers' as recited above, which clearly hold the output of the previous stage)(Inoue clearly shows in Figure 7 that the latches 251-253 are serially connected and that their results are passed to each other, where it is clear that a serial connection is advantageous. See also latches 254-256 in Figures 8-10)

-A logic circuit for performing a logic operation with respect to all bit data set in said clip registers and setting a clip flag indicating whether or not a vertex to be judged is inside or outside the multi-dimensional region of the object to be drawn. (Negishi teaches element 307, Figure 3, the clip state code generator is clearly "a logic circuit" and it performs operations on the clip codes to generate clip state codes (7:52-8:25). Further, Figure 5(a) provides an example of how that portion of the system works (8:27-47), where the clip state codes indicate whether an object is inside or outside the clip region as explained therein. Further, the fourth embodiment shown in Figure 10 has a mask register 1001 that is explicitly taught to perform logical operations against the entire contents of the target register in terms of a comparison operation (see 11:15-60))(Inoue teaches element 26 (primitive selection circuit) that generates signal M2, which

Art Unit: 2628

represents the clip flag concerning whether or not the vertex is judge to be inside or outside the multi-dimensional region of the object to be drawn.)

Reference Negishi therefore teaches most of the limitations of the instant claim as set forth above except for stating explicitly that the vertex is compared with both the judgment value and a negative judgment value, and the cascaded shift register combination per se. However, one of ordinary skill in the art would appreciate that the judgment values merely define the bounding region of the two- or three-dimensional region or volume, and that if the coordinate system were normalized so that the zero value and/or origin was situation within the clipping region or volume. One of ordinary skill in the art at the time the invention was made would understand that such a modification would be trivial and could be advantageous since it would reduce the amount of processing necessary to perform the comparisons. In any case, the limitation of negative judgment value is truly irrelevant because the values of such judgment values is entirely dependent upon the coordinate system used and the bounding region defined by such a system, which may not be symmetric and/or axisymmetric. Therefore, since the system of Negishi generates judgment value results for at least positive vertices, it would be obvious to do so for both upper and lower bounds as tested for by XMIN, XMAX, and the like.

Further, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the second embodiment of Negishi such that it had the mask register in the fourth embodiment, so that the masking and comparison could

be performed in such a way that allowed for conditional judgments and jump instructions to be used, which would clearly give it more flexibility.

Additionally, Negishi teaches above the use of clip state codes that are output with the clip codes the constitute the judgment values that are required, where the comparisons are done based on these values and meet the limitations of the instant claim. At the least, such modification to do both comparisons would have been obvious in light of the reference as explained above, since both the min and max are tested against judgment values (e.g. clipin, clipout (in region and out of region)) anyway, where this constitutes the key idea of two tests with respect to the clip codes.

However, Negishi does not directly teach the use of a current clip register, although it certainly suggests such, since the results from the clip code generator circuits are sent to shift registers that store the results and then shift results out, while the resultant data values are held in clip register 308, which also contains clip state codes. It is noted that Negishi clearly teaches that such data is passed from the shift registers **to the clip register**, which is clearly in a serial connection. Clearly, this constitutes two shift registers. Next, Inoue also suggests the use of such techniques, as illustrated in elements 251, 252, and 253, which serve as registers given how they are connected and how they function for the second embodiment (6:35-7:50), where they store the results of the calculation (in the same manner as register 308 of Negishi), but perform logical operations upon the contents of those registers, such that they can then be selected easily as required by the dimension selection (e.g. the determination of

Art Unit: 2628

what type of primitive was being used, which is obviously advantageous for the reasons set forth below.)

Inoue teaches that each type of primitive would take one more set of shift registers (e.g. three primitive types – one, two, or three points or vertices requiring 6, 12, or 18 bits respectively), it would be obvious to disable or enable registers based on the processing power required (e.g. the size of the primitive to be processed). The type of primitive would be selected during vertex processing and the appropriate shift registers would be enabled or disabled by the control circuit. Therefore, it would have been obvious to use the control circuitry blocks (elements 251-253 in Figure 7, elements 254-256 in Figures 8 and 9), and the like – and have cascaded registers of the type shown in Negishi, with the large register 308 replaced by the smaller registers / memories of Inoue so that only necessary circuits are utilized and that for a point primitive unnecessary calculations and the like are not made.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the clipping circuit of Negishi with the absolute values of Inoue, since Inoue is clearly designed to accommodate N dimensions (2:41-49) where Negishi is meant to only accommodate standard (x, y, z) coordinates in the cited embodiment, and clearly Inoue further enables faster processing depending on the type of primitive, as stated above

Additionally, it is pointed out that although Negishi and Inoue operate on plural vertices, the CAFC has held (see *Scanner Technologies v. IKOS Vision systems* (CAFC

2004)) repeatedly that the article 'a' is construed as 'one or more', which therefore means that these references cover this particular grounds of rejection.

As to claim 2, clearly as shown in Figures 5(a)-5(b) and 6 and as explained above in 7:52-8:16, the system of Negishi utilizes coordinates of vertices in 3-space, that is utilizes a three-dimensional coordinate system, and such vertices therefore correspond to a plurality of coordinate axes. Clearly, as explained in 8:15-10:20 in the example provided for Figures 6 and 7, the clip codes generated by FPUs 103-105, clearly constitute a 'plurality of clip codes' that do correspond to the coordinate axes. Clearly since such clip codes are then output to shift registers 304-306, the clip registers must inherently have a capacity for holding at least those clip codes, as recited in the cited sections, as discussed in the rejection to the parent claim above, and it would be obvious.

As to claim 3,

A clipping device as set forth in claim 1, wherein said clip code generation circuit generates said clip codes based on code data obtained by subtracting an absolute value of said judgment reference value from the absolute value of said vertex coordinates, code data of said vertex coordinates, and code data of said judgment reference value.

Reference Negishi does not explicitly teach the use of an absolute value operator, but does teach the setting of a target volume with the area around it, and the

Art Unit: 2628

checking of a vertex to see if it is in the test volume and within the clip volume and the setting of flags thereof. Reference Inoue teaches the use of absolute values in clipping preprocessing circuits, specifically 2:19-41 teaches that the clipping device performs an operation (subtraction) on the absolute value of a vertex coordinate and a pair of boundaries, wherein similar to Negishi the clip data of the boundaries are put into the register and the check is performed, and the code data recited by applicant clearly is stored (from the axis basis). Further, Table 1 in Inoue illustrates (1:53-63) how codes are created for the view volume. It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the clipping circuit of Negishi with the absolute values of Inoue, since Inoue is clearly designed to accommodate N dimensions (2:41-49) where Negishi is meant to only accommodate standard (x, y, z) coordinates in the cited embodiment.

As to claim 4,

A clipping device as set forth in claim 2, wherein said clip code generation circuit said clip codes based on code data obtained by subtracting an absolute value of said judgment reference value from the absolute value of said vertex coordinates, code data of said vertex coordinates, and code data of said judgment reference value.

See the rejection to claim 3 above. The additional limitations of claim 2 are all taught by the primary reference as discussed in the rejection of claim 2. The claim wording is the same with the substitution of only "claim 2" for "claim 1". Therefore, the

entirety of that rejection, along with the motivation and combination, is incorporated herein by reference without further comment.

As to claim 5,

A clipping device for judging whether or not vertices of a primitive expressed by a predetermined coordinate system are inside or outside a multi-dimensional region of an object to be drawn, a polyhedron being drawn in units of primitives including a plurality of vertices, comprising: (preamble ignored as per *In re Hirao* and *Kropa v. Robie*, as it only recites an intended use, and the claimed process steps or apparatus parts can stand by themselves and perform the intended function. Secondly, the system of Negishi clearly teaches in the abstract that the system is intended to operate in three-dimensions, and the examples shown in Figures 4 and 6 for example show three-dimensional coordinate space, and clearly a three-dimensional object would be composed of triangles or the like, and clearly Negishi teaches as set forth below processing this kind of item, and in Figures 4 and 6 such triangles are shown.)

-A clip code generation circuit for generating clip codes obtained by setting data in accordance with results of a comparison of vertex coordinates of said primitive and a judgment reference value of said multi-dimensional region and a negative value of the judgment reference value as bit data for the amount of the vertexes of the primitive; (Negishi in Figure 3 teaches a clip code generating circuit, where FPU (floating point units) 103, 104, and 105 generate clip codes (7:52-8:15) that then are passed to shift registers 304, 305, and 306. As set forth (7:52-8:15) by Negishi, the clip codes are

Art Unit: 2628

generated by comparing the coordinates of the vertices and the reference values (e.g. $X=X_{MAX}$ and $X=X_{MIN}$) for comparison through the clipping region (which *prima facie* is multi-dimensional (see Figures 5-7 and the explanations provided in the cited references, and these are clearly bit data since they are in the memory of a digital computer. It would be obvious, as shown in Figure 6 and further explained in 8:64-10:7, that each vertex is processed on its own, which teaches vertices, and the recited 'judgment values' are merely the bounding coordinates of the clipping region and/or the guardband. Further, clearly the examples of Negishi teach that a primitive (e.g. a triangle) is processed by the number of vertices, in this case three, and clearly the embodiment shown in Figure 1 shows that a four-vertex version is used (6:15-56); indeed, in 7:30-48 it states that any number of FPU's can be used to accommodate any number of vertices or the like) (Inoue, registers 23 in Figure 8 for example)

-A current clip register for a shifting the clip codes generated at said clip code generation circuit in accordance with a control signal; (Koss 9:38-51 discloses vertex clip code shift registers, which *prima facie* perform the recited functionality, since clip codes are *prima facie* generated by a clip code generating circuit and, if necessary, moved utilizing the clip code bus disclosed earlier. However, more specifically, Fig. 7 shows a shift register wherein coordinates are shifted in response to a control signal (12:30-60) and discloses how clip codes are shifted in that manner as well)(Inoue teaches registers for this processing in 2:19-41.)

-Clip registers of at least a number smaller than the number of vertexes of said primitive by one cascade connected to an output of said current clip register and able to replace

Art Unit: 2628

the held data with the clip codes held by the register of a previous stage in accordance with a control signal; (Prima facie, shift instructions within the shift register that overwrite other coordinates or flags in that same register act as replacement operations.) (Inoue clearly shows in Figure 7 that the latches 251-253 are serially connected and that their results are passed to each other, where it is clear that a serial connection is advantageous. See also latches 254-256 in Figures 8-10, where Inoue allows the dimensionality of the primitive to determine the number of clip registers extant, as discussed below)

-A control circuit for outputting said control signal to the current clip register when receiving a clip code generation instruction to shift the clip codes generated at said clip code generation circuit and outputting said control signal to a corresponding clip register so as to replace the clip codes between adjacent clip registers including said current clip register when receiving a replacement instruction; (As discussed in the above paragraph, Koss 9:38-51 discusses the operation of such shift registers, which includes moving data as illustrated in Fig. 7 and structurally discussed in 9:51-58 (that is, that fulfills the adjacent shift register limitation (shown in Fig. 7) and the clip register limitation in general). The vertex load control line 224 for shift-registers (234, 236, 238, 240, 242, and 323, Koss Fig. 4) can be driven by the left stack control unit 122 – Koss Fig. 3) (10:1-24). Also, under some circumstances the shift registers can be controlled by the trivial accept and reject circuit shown below the shift registers in Fig. 4. Either the left stack control unit 122 or the accept/reject logic 250 in Fig. 4.) (Prima facie, shift instructions within the shift register that overwrite other coordinates or flags in that same

Art Unit: 2628

register act as replacement operations.)(Koss Figure 10 a flowchart of steps is shown. As the systems transitions from step 312 to 316 and complete processing a vertex, a flag is generated internally. Further, once step 316 is complete, the system generates results flag for all vertices (step 318). Koss further teaches in 6:31-47 that a replace mode can exist that will substitute one set of color values (object) for another (texture). Such a replace mode *prima facie* could obviously be applied to coordinates instead of colors (three values (x, y, z) (R, G, B)). Such replacement mode as discussed above would obviously be applied then, or if only one set of registers was being used, would be applied in between steps 312 and 316 in Koss if only one register were being used (and applicant's claim specifically states that it includes situations where only one register would be used.)(The resulting clip codes from FPU 103, 104, and 105 are then sent to shift registers 304, 305, and 306 that are comparable to applicants "clip registers". The results are then passed on to generic clip code register 308. The system works as specified above (8:48-64).)

-A logic circuit for performing a logic operation with respect to all bit data set in said clip registers and setting a clip flag indicating whether or not a vertex to be judged is inside or outside the multi-dimensional region of the object to be drawn. (Element 307, Figure 3, the clip state code generator is clearly "a logic circuit" and it performs operations on the clip codes to generate clip state codes (7:52-8:25). Further, Figure 5(a) provides an example of how that portion of the system works (8:27-47), where the clip state codes indicate whether an object is inside or outside the clip region as explained therein. Further, the fourth embodiment shown in Figure 10 has a mask register 1001 that is

explicitly taught to perform logical operations against the entire contents of the target register in terms of a comparison operation (see 11:15-60))(Inoue teaches element 26 (primitive selection circuit) that generates signal M2, which represents the clip flag concerning whether or not the vertex is judge to be inside or outside the multi-dimensional region of the object to be drawn.)

Reference Negishi teaches most of the above limitations, but does not expressly teach the limitation concerning the current clip register (although implicitly the common clip register 308 could partially fulfill that purpose, but that is beside the point).

Reference Inoue teaches the additional limitations as set forth above.

However, one of ordinary skill in the art would appreciate that the judgment values merely define the bounding region of the two- or three-dimensional region or volume, and that if the coordinate system were normalized so that the zero value and/or origin was situation within the clipping region or volume. One of ordinary skill in the art at the time the invention was made would understand that such a modification would be trivial and could be advantageous since it would reduce the amount of processing necessary to perform the comparisons. In any case, the limitation of negative judgment value is truly irrelevant because the values of such judgment values is entirely dependent upon the coordinate system used and the bounding region defined by such a system, which may not be symmetric and/or axisymmetric. Further, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the second embodiment of Negishi such that it had the mask register in the fourth embodiment, so that the masking and comparison could be performed in such a way

that allowed for conditional judgments and jump instructions to be used, which would clearly give it more flexibility.

Further, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the second embodiment of Negishi such that it had the mask register in the fourth embodiment, so that the masking and comparison could be performed in such a way that allowed for conditional judgments and jump instructions to be used, which would clearly give it more flexibility.

Additionally, Negishi teaches above the use of clip state codes that are output with the clip codes that constitute the judgment values that are required, where the comparisons are done based on these values and meet the limitations of the instant claim. At the least, such modification to do both comparisons would have been obvious in light of the reference as explained above, since both the min and max are tested against judgment values (e.g. clipin, clipout (in region and out of region)) anyway, where this constitutes the key idea of two tests with respect to the clip codes.

However, Negishi does not directly teach the use of a current clip register, although it certainly suggests such, since the results from the clip code generator circuits are sent to shift registers that store the results and then shift results out, while the resultant data values are held in clip register 308, which also contains clip state codes. It is noted that Negishi clearly teaches that such data is passed from the shift registers **to the clip register**, which is clearly in a serial connection. Clearly, this constitutes two shift registers. Next, Inoue also suggests the use of such techniques, as illustrated in elements 251, 252, and 253, which serve as registers given how they are

connected and how they function for the second embodiment (6:35-7:50), where they store the results of the calculation (in the same manner as register 308 of Negishi), but perform logical operations upon the contents of those registers, such that they can then be selected easily as required by the dimension selection (e.g. the determination of what type of primitive was being used, which is obviously advantageous for the reasons set forth below.)

Inoue teaches that each type of primitive would take one more set of shift registers (e.g. three primitive types – one, two, or three points or vertices requiring 6, 12, or 18 bits respectively), it would be obvious to disable or enable registers based on the processing power required (e.g. the size of the primitive to be processed). The type of primitive would be selected during vertex processing and the appropriate shift registers would be enabled or disabled by the control circuit. Therefore, it would have been obvious to use the control circuitry blocks (elements 251-253 in Figure 7, elements 254-256 in Figures 8 and 9), and the like – and have cascaded registers of the type shown in Negishi, with the large register 308 replaced by the smaller registers / memories of Inoue so that only necessary circuits are utilized and that for a point primitive unnecessary calculations and the like are not made.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the clipping circuit of Negishi with the absolute values of Inoue, since Inoue is clearly designed to accommodate N dimensions (2:41-49) where Negishi is meant to only accommodate standard (x, y, z) coordinates in the cited

embodiment, and clearly Inoue further enables faster processing depending on the type of primitive, as stated above

Additionally, it is pointed out that although Negishi and Inoue operate on plural vertices, the CAFC has held (see *Scanner Technologies v. IKOS Vision systems* (CAFC 2004)) repeatedly that the article 'a' is construed as 'one or more', which therefore means that these references cover this particular grounds of rejection.

As to claim 6,

A clipping device as set forth in claim 5, wherein said control circuit outputs said control signal to a corresponding clip register so as to replace the clip codes along with the vertex processing in accordance with the type of the primitive.

Reference Negishi does not explicitly teach this limitation. Reference Inoue teaches in 1:40-67 and 2:1-11 that different amounts of memory (registers) are required for processing each kind of primitive. Inoue teaches that each type of primitive would take one more set of shift registers (e.g. three primitive types – one, two, or three points or vertices requiring 6, 12, or 18 bits respectively), it would be obvious disable or enable registers based on the processing power required (e.g. the size of the primitive to be processed). The type of primitive would be selected during vertex processing and the appropriate shift registers would be enabled or disabled by the control circuit (Koss 10:24-44) as required, which occurs during the initial vertex processing stage. Finally, Inoue has a dimension selection signal that would perform this function (11:25-32). . It would have been obvious to one having ordinary skill in the art at the time the invention

Art Unit: 2628

was made to combine the clipping circuit of Negishi with the absolute values of Inoue, since Inoue is clearly designed to accommodate N dimensions (2:41-49) where Negishi is meant to only accommodate standard (x, y, z) coordinates in the cited embodiment, and clearly Inoue further enables faster processing depending on the type of primitive, as stated above.

As to claim 11,

A clipping device as set forth in claim 5, wherein:

- Said coordinates of said vertexes include values corresponding to a plurality of coordinate axes of a predetermined coordinate system,
- Said clip code generation circuit generates a plurality of clip codes corresponding to the coordinate axes, and
- Said clip registers have capacities for holding at least said plurality of clip codes.

See rejection to claim 2. Claim 11 is an exact duplicate of claim 2, and the only difference is the substitution of the words "claim 5" for "claim 1". The rejection is based only on the primary reference anyway.

As to claim 12,

A clipping device as set forth in claim 5,

- Wherein the clip code generation circuit generates said clip codes based on code data obtained by subtracting an absolute value of said judgment reference value from the absolute value of said vertex coordinates, code data of said vertex coordinates, and code data of said judgment reference values.

See rejection to claim 3. Claim 12 is an exact duplicate of claim 3, and the only difference is the substitution of the words "claim 5" for "claim 1". Therefore, the explanation, motivation, and combination are incorporated herein by reference without further comment.

Claims 7-8 are rejected under 35 USC 103(a) as unpatentable over Negishi in view of Inoue as applied to claim 5 above, and further in view of Koss.

As to claims 7 and 8,
Wherein said control circuit generates a vertex ready flag indicating that the vertexes' worth of clip codes of said primitive are ready at the time of the replacement instruction.

Negishi and Inoue fail to teach the vertex ready flag as recited above. Reference Koss does not explicitly teach this limitation, but in Figure 10 a flowchart of steps is shown. As the systems transitions from step 312 to 316 and complete processing a vertex, a flag is generated internally. Further, once step 316 is complete, the system generates results flag for all vertices (step 318). Koss further teaches in 6:31-47 that a replace mode can exist that will substitute one set of color values (object) for another (texture). Such a replace mode *prima facie* could obviously be applied to coordinates instead of colors (three values (x, y, z) (R, G, B)). Inoue 8:9-23 teaches that vertices are updated, that is, overwritten at a particular signal. Such replacement mode as discussed above would obviously be applied then, or if only one set of registers was being used, would be applied in between steps 312 and 316 in Koss if only one register were being used (and applicant's claim specifically states that it includes situations

where only one register would be used).) Further, a replacement mode could also be construed as occurring when the register values are shifted to generate the clip sub-does, as shown in Fig. 7 of Koss.

Reference Negishi teaches most of the above limitations, but does not expressly teach the limitation concerning the current clip register. Reference Koss teaches the additional limitations as set forth above. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Negishi with Koss because the system of Koss significantly reduces computational load for primitives and other advantages (3:15-55), the Koss reference is analogous art, and can handle polylines (4:20-35), which would allow the Negishi reference to handle N vertices in a way that would be computationally easier than dividing N primitives into N shift registers as per Negishi's suggestion.

As to claim 8,
See the rejection for claim 7, wherein this claim is the same limitation but dependent upon claim 6. However, the same combination of references above (Negishi in view of Inoue) is used to reject claim 6. Therefore, the same rejection valid upon claim 7 is equally valid for and upon claim 7.

Claims 9-10 are rejected under 35 U.S.C. 103(a) under Negishi in view of Inoue as applied to claims 5 and 6 above, and further in view of Oliver et al (US 5,313,610)('Oliver').

As to claims 9 and 10,

Wherein said control circuit selectively initializes a desired register among a plurality of clip registers including said current clip register under predetermined conditions.

References Negishi and Inoue do not explicitly teach this limitation. Reference Oliver teaches (3:58-67) that registers are selected and initialized through a bus, meaning that such registers can be individually selected and initialized. As shown in Oliver Fig. 2, the registers (40₁-40_k) are controlled by control logic 20 over said bus 14. It is well known in the art to initialize a register to prepare it for use in computational purposes or during a reset. Obviously, the control circuit of Oliver could perform the recited limitation of claim 9, since the clipping circuits of Inoue have multiple registers, including the "current clip register" recited by applicant as established in the rejections to earlier, parent claims. Inoue 8:9-23 teaches that vertices are updated, that is, overwritten at a particular signal), these would constitute circumstances that would generate "predetermined conditions" as recited by applicant. Given that Oliver teaches a control circuit for memory systems, e.g. register files, and Inoue has multiple registers that could *prima facie* obviously be embodied as a register file, it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the clip circuits of Koss and Inoue with the control logic of Oliver to achieve the selective initialization recited by applicant.

Reference Negishi teaches most of the above limitations, but does not expressly teach the limitation concerning the current clip register. Reference Oliver teaches the additional limitations as set forth above. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Negishi/Inoue with Oliver

Art Unit: 2628

for at least the reason that the system of Oliver significantly circuit complexity and generates addresses more quickly (2:8-30, 3:20-40).

As to claim 10, this claim is dependent upon claim 6, but otherwise is the same as claim 9. However, Negishi and Inoue are used to reject claim 6 as well, which is incorporated by reference. The remaining limitation is identical to that of claim 9, and is incorporated along with the motivation from the rejection to that claim above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Woods whose telephone number is 571-272-7775. The examiner can normally be reached on M-F 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2628

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Eric Woods

2/20/2006



MICHAEL RAZAVI
SUPERVISORY PATENT EXAMINER
MICHAEL RAZAVI